DPM® 3SE DIAGNOSTICS GUIDE

DPM® 3 diagnostics are a collection of test routines which can quickly verify the health of the DPM 3 components. If any problems are found, the tests display information which will allow a technician to quickly isolate and correct the problem. These diagnostics can be executed any time a problem is suspected in the DPM 3. It is also a good idea to run diagnostics after any service work (such as Sample RAM upgrade), to verify operational status. This document leads the technician through execution of the diagnostics, interpretation of the results, and isolation of the cause of failure.

The diagnostics disk is available to end-users of the DPM 3, as an aid in verifying operational status. If a problem is detected, the user should not attempt a repair. Repair should be performed by Peavey Factory Authorized Service Centers.

RUNNING DIAGNOSTICS

The key combination 'Pause-Erase' causes the machine to enter into diagnostics mode. This brings up a CAUTION screen, warning the user that RUNNING DIAGNOSTICS WILL DESTROY ALL DATA in Program RAM, Effects RAM, Sequencer RAM, System RAM, and Sample RAM. If there is data you need to save, or if you want to exit now for any reason, just press any non-soft key to return to normal operating mode. If you exit now, there will be no damage done to any data. If 'continue' is selected, a test is performed on Sequencer RAM. (The diagnostics disk should be in the drive before pressing the -cont- softkey.)

If the Sequencer RAM test fails, the results of the failed test will be displayed, and there will be no attempt to load the rest of the diagnostics off of the disk. You can return to normal operation by hitting any non-soft key. If the Sequencer RAM test passes, an attempt is made to load the file "DIAGNOSE.DPM" from disk. The disk is automatically searched for the diagnostics file.

Once the diagnostics are loaded, control is passed to the code loaded in sequencer RAM, and the main diagnostics menu appears.

```
Selct: AllMem WvMem FxRAM PgRAM SysRAM
-exit-              Batt    MIDI FPanel
```

'AllMem' is a memory verification test which performs all four of the other memory tests in sequence.

'WvMem' performs testing on Wave ROM, Sample RAM, DSP1, and DSP2.

'FxRAM' tests Effects RAM and the Effects DSP.

'PgRAM' performs testing on Program memory, where programs 1-100 are stored.

'SysRAM' performs testing on System RAM, where internal data is stored.

'Batt' displays the voltages of the system battery and cartridge battery.

'MIDI' verifies that the MIDI interface is in working order.

'FPanel' is an interactive test which allows the user to exercise front panel devices and to see the data values which are generated.

Choose any test, and wait for the results. It is wise to run the Front Panel test last, since there is no return from this test. After completing the interactive front panel test, the machine must be turned off and back on to return to the normal operating system. After running any of the other tests (besides Front Panel), it is possible to return to the normal operating system via the -exit- softkey. AFTER RUNNING DIAGNOSTICS, THE DPM 3 MEMORY SHOULD ALWAYS BE RE-INITIALIZED, using the "Multi-Pause" procedure outlined in the DPM 3 user's manual. In order to use the machine again, you should then load programs, effects, and sequences from disk.

INTERPRETING RESULTS

If one of the memory tests fails, the failed test will be identified, and a data mask will be displayed, along with the number of errors which occurred. The data mask will be a hexadecimal representation of a binary mask in which each good data bit is represented by a '1', and each bad data bit is represented by a '0'. To determine which memory chip to replace, look at the data mask.

A) In the case of Sequencer RAM, each half of the mask represents one of the Sequencer RAM chips. The least significant (right) half of the mask corresponds to the "Seq RAM Lo" chip, and the most significant (left) half of the mask relates to the "Seq RAM Hi" chip. A value of 'FF' in either of these positions indicates a good chip. Any value other than 'FF' indicates some sort of a problem.

B) In the cases of Program RAM and System RAM, the results are displayed in the same format as for Sequencer RAM. System RAM and Program RAM share two memory chips. If there is a failure of a data line diagnosed by the System RAM test, it is likely that the Program RAM test will show the same thing. In either case, it is possible to tell which chip is failing by noticing which half of the data mask contains a non-'FF' value.

C) The Effects RAM test displays a different results format, but the data mask is interpreted in the same way as the data masks for the Sequencer, Program, and System RAM tests. The only difference is that the Effects RAM mask represents 24 bits instead of 16 bits.

The first two hex digits (the most significant byte) of the mask correspond to the "FX RAM Hi" chip. The middle two hex digits of the mask correspond to the "FX RAM Lo" chip. The last two digits represent addressing hardware, and should always be 'FF'. In addition to the data mask, the Effects RAM test supplies an address mask and complemented address mask. These two masks are interpreted in the same manner as the data mask.

If both the "FX RAM Hi" byte and the "FX RAM Lo" byte of the masks indicate errors, or if either the 'int' or 'SSI' field is not 'O.K.', then it is likely that there is a problem with the Effects DSP.

D) The Wave Memory Test checks both Wave ROM and Sample RAM, and tests both DSP 1 and DSP 2. If there is a communication problem between the main processor and either of the DSP's, a 'DSPcom error' screen will be displayed. This screen will tell you whether DSP1, DSP2, or both DSP's failed in commmunication.

There are up to eight screens of data presented as detailed test results for the Wave Memory test. The first two screens present interrupt counts and ROM checksums for DSP 1. The third screen presents the first page of RAM checksums. If there are more RAM checksums applicable for the type of memory chips being tested, then the next three pages will show the remaining RAM checksums. The last two screens present the results of the test performed by DSP 2. This will help to narrow down any problem with one of the DSP chips.

The 'int' and 'SSI' fields should contain 'O.K.' on both the DSP1 and the DSP2 page. Any other values signify that the test failed. (The 'Lo cksum' field should always be zero.)

On the checksum pages, all checksums should be 'O.K.'. Any other value represents a bad memory chip. If ALL checksum values are bad, it is probably due to a bad DSP. In particular, if the ROM checksums are 'O.K.' for one DSP, and not for the other, then it is definitely a problem with the DSP chip (or the connections to the DSP chip). Note that the RAM test is not perfomed by DSP 2, and so there are no RAM checksum pages for DSP 2.

E) The All Memory test simply invokes the System RAM, Program RAM, Effects RAM, and Wave Memory tests in sequence. If there are any failures, the test will stop, and the first error encountered will be displayed. If there are no errors, the test will end at the Wave Memory Test completion screen.

F) The Battery Test simply reads the voltages of the System battery and the Cartridge battery (if there is a RAM cartridge inserted), and displays the voltages onscreen. Typical voltages are around 3.8 - 4.0 Volts for the system battery, and 2.7 - 2.9 Volts for the cartridge battery. Note that the Cartridge Battery is contained in the RAM Cartridge itself, and is not an integral part of the DPM 3 hardware.

G) The MIDI Test requires external connection of a MIDI cable from the DPM 3 'MIDI OUT' port to the DPM 3 'MIDI IN' port. The MIDI Test simply sends a stream of MIDI data (consisting of all the values 00 - FF) out the MIDI OUT port, and expects to get the same stream back in the MIDI IN port. If there is any discrepancy, the test fails. If there is no discrepancy, the test passes, and the average time interval between bytes is displayed in microseconds. A typical value for this interval would be 328 microSeconds.

H) The Front Panel Test is a test run by the Front Panel Processor itself. The test verifies the interface to all the buttons, input devices, and serial ports. After selecting 'FPanel' from the main diagnostics menu, it takes a second or two for the front panel processor to enter into diagnostics mode. TOUCHING ANY BUTTONS WHILE THE FRONT PANEL TEST IS BEING SET UP MAY CAUSE TERMINATION OF THE TEST, with a message about shorts being found.

Once Front Panel Test Mode is entered, there are four tests which may be selected.

1) The SWITCH TEST allows for the user to check each switch for closure. The switch location is displayed for closure verification.

2) The ANALOG DEVICE TEST displays the value (0-255) and the device code for the analog devices (Volume and Data Sliders, Pitch and Mod wheels, Aftertouch strip, and Volume Pedal) when movement is detected.

3) The DATA WHEEL TEST displays information on movement of the data wheel (left or right).

4) The SERIAL I/O TEST requires a special jumper which cannot be installed without opening the unit. This test should not be performed in the field.

NOTE: The SERIAL I/O TEST is unnecessary when Front Panel Test is entered through the Diagnostics menu. If the Front Panel Test mode is successfully entered, then the Front Panel Serial I/O interface must be working.

TROUBLESHOOTING

This section provides details on how to interpret error screens, and what to do to correct the problem.

NOTE: THE POWER SHOULD ALWAYS BE OFF BEFORE ATTEMPTING REMOVAL OF ANY CABLES, BOARDS, or CHIPS, etc. In addition, all IC's should be considered 'static sensitive', and should be handled as such to prevent damage.

A) SEQUENCER RAM

Sequencer RAM test failure screens can be interpreted as follows:

```
Failed          xxxx errs  data:xxxx
xxxx test                          -ret-
```

1) On the far left side of the screen, the test which failed is displayed. There are actually four tests performed.

a) ONES TEST - writes ones into all of sequencer RAM, and then reads them back. The ONES TEST is designed to identify any data bits Stuck At Zero. Failure of the ONES TEST, since it is the first test run, may also indicate address line problems, such as an addressing pin not seated properly in the socket.

b) ZERO TEST - writes zeroes into all of sequencer RAM, and then reads them back. The ZERO TEST is designed to identify any data bits Stuck At One.

c) WALK TEST - 'walks' a one through each bit of sequencer RAM. The WALK TEST is designed to assure that no data lines are tied together.

d) RAMP TEST - writes a test word to each address, incrementing that test word by 1 (creating a 'ramp' function) for each word. The RAMP TEST is designed to assure that no address lines are unconnected or tied together.

Upon failure of any of these tests, the failed test will be identified, and a data mask will be displayed, along with the number of errors which occurred. The data mask will be a hexadecimal representation of a binary mask in which each good data bit is represented by a '1', and each bad data bit is represented by a '0'. The number of errors is also displayed in hexadecimal, and represents the number of tested locations which yielded an error. There are 32,768 16-bit words of sequencer RAM, and so the largest possible number of failures is 32,768, or 8000 hexadecimal.

In the case of Sequencer RAM, each half of the mask represents one of the Sequencer RAM chips. The least significant (right) half of the mask corresponds to the "Seq RAM Lo" chip, and the most significant (left) half of the mask relates to the "Seq RAM Hi" chip. A value of 'FF' in either of these positions indicates a good chip. Any value other than 'FF' indicates some sort of a problem.

EXAMPLES:

1) A broken lead on pin 19 (the most significant data line) of the "Seq RAM HI" chip would result in the following screen:

```
Failed          8000 errs     data:7FFF
Zero test
```

Note that the most significant bit in the mask (0111 1111 1111 1111) is a zero, representing a bad reading from that bit. 8000 errs tells you that every test location failed, which we would expect when a data line is bad. The solution to this problem is

to replace the "Seq RAM Hi" chip. If, after replacing the offending chip, the test still fails, it is likely that some connection to that chip is failing.

2) Improper seating of the "Seq RAM HI" chip, causing pin 1 (the most significant address line) to dangle out of the socket, would result in the following screen:

Failed Ramp test	4000 errs	data:00FF

Noting that the failed test is the RAMP TEST, we know that the ONES, ZERO, and WALK test all passed. (If any of them had failed, we would never have even reached the RAMP TEST. Note that the least significant half of the mask (0000 0000 1111 1111) is all ones, meaning no errors from the "Seq RAM Lo" chip. This tells us that there is an addressing problem somewhere in the "Seq RAM Hi" chip.

The solution to this problem is to reseat the "Seq RAM Hi" chip, making sure that all pins are correctly inserted into the socket.

3) A faulty solder connection of the "Seq RAM Lo" socket to the main processor board at pin 28 (chip power) would result in the following screen:

Failed Zero test	8000 errs	data:FF00

Since there are 8000 (hex) errors, we know that the data lines are not working properly. However, since no data bits at all showed up good in the least significant half of the mask (1111 1111 0000 0000), we suspect that the chip is not working at all.

The solution to this problem is to replace the "Seq RAM Lo" chip. After running the test again, and getting the same results, we suspect not the chip, but the connections to the chip. Checking power to the chip with a voltmeter, we find that +5 Volts is not reaching pin 28 of the chip. The problem is with the board itself.

B) SYSTEM RAM (& PROGRAM RAM)

If there is a problem with your System RAM, it is unlikely that your machine will run long enough to perform this test; but it's possible. Inability of the system to power up correctly may be caused by a problem with the System RAM chip; however, this is just one possible cause of that problem.

System RAM test failures can be interpreted as follows:

1) On the far left side of the screen, the test which failed is displayed. The four tests performed are identical to those described above for Sequencer RAM.

Interpretation of the data mask for the System RAM test is identical to that for the Sequencer Ram test. The maximum possible number of errors, however, is only 4000 (hex), as compared to 8000 for Sequencer RAM. (System RAM test is performed on only 32K bytes.)

2) System RAM and Program RAM share two memory chips. If there is a failure of a data line diagnosed by the System RAM test, it is likely that the Program RAM test will show the same thing. In either case, it is possible to tell which chip is failing by noticing which half of the data mask contains a non-'FF' value.

C) EFFECTS RAM

Effects RAM is actually tested by the Effects DSP processor. If there is a communication problem between the main processor and the Effects DSP, the memory test cannot be performed, and a 'DSP com error' screen will be displayed.

Effects RAM failures can be interpreted as follows:

```
ints: xxxx     xxxx errs     data:xxxxxx
SSI:  xxxx     adr:  xxxxxx  -adr:xxxxxx  -ret-
```

1) On the far left of the results screen is an interrupt status for the effects DSP chip. If either 'ints' or 'SSI' contains a value other than 'O.K.', there may be a problem with the DSP chip. A signed numerical value in this field denotes a deviation in the number of interrupts received during the test compared to the expected number of interrupts. Any deviation in this number is an indication of a possible problem with the Effects DSP, or with the system clock crystals.
2) In the center of the screen, on the top line is a count of errors. If there are more than 'FFFF' (hex) errors, the word 'many' is displayed.
3) On the right side of the top line is a data mask, similar to the mask seen in the Sequencer RAM, System RAM, and Program RAM tests. This mask, however, is a 24-bit mask, since the DSP uses 24-bit words. The first two hex digits (the most significant byte) of the mask correspond to the "FX RAM Hi" chip. The middle two hex digits of the mask correspond to the "FX RAM Lo" chip. The last two digits represent addressing hardware, and should always be 'FF'.
4) On the bottom line are two more masks, derived from 1) writing the address of each location into that location, and 2) writing the complement of the address (-adr) of each location into that location. A non-'FF' value in any byte of any of the three masks indicates a problem with the corresponding memory chip. ("FX RAM Hi" for the first two digits, "FX RAM Lo" for the middle digits.)

EXAMPLES:

1) A non-functional "FX RAM Lo" chip would result in the following screen:

```
ints:O.K.    many errs    data:FF00FF
SSI: O.K.    adr:FF00FF   -adr:FF00FF   -ret-
```

Note that the middle word of the mask (1111 1111 0000 0000 1111 1111) is all zeroes, representing a bad reading from all bits of "FX RAM Lo". The solution to this problem is to replace the "FX RAM Lo" chip.

2) A non-functional "Effects DSP" chip would result in the following screen (or something similar):

```
ints:-080C7  many errs    data:F948DE
SSI: none    adr:750B14   -adr:90CEAD   -ret-
```

Noting that everything looks pretty bad, including the interrupt status, we suspect the DSP chip is not functioning properly.

The solution to this problem is to replace the "Effects DSP" chip. Be sure to use the correct tool when removing the DSP chip to avoid damage to the socket.

3) A clock crystal which oscillates slower than most could cause test failure, resulting in the following screen:

ints:-00007	0000 errs	data:FFFFFF	
SSI: O.K.	adr:FFFFFF	-adr:FFFFFF	-ret-

Note that everything looks pretty good, except for the interrupt count. This probably means that one of the two clock crystals is out of tolerance.

The solution to this problem is to replace one of the clock crystals. Try the 16 MHz clock crystal first. If the problem persists, replace the 27 MHz clock crystal.

D) WAVE MEMORY

The Wave Memory Test checks both Wave ROM and Sample RAM, and, in doing so, effectively tests both DSP 1 and DSP 2, as they are used to perform the memory tests. If there is a communication problem between the main processor and either of the DSP's, a 'DSPcom error' screen will be displayed. This screen will tell you whether DSP1, DSP2, or both DSP's failed in commmunication.

As there are different Sample RAM configurations installable in the DPM 3, the Sample RAM Test can only verify the amount of RAM which tests as good. For example, if you have 128K Sample RAM installed, the Wave Memory test might pass, and display the message '64K RAM approved.' This means that there was an error in the upper 64K of Sample RAM. There is no way for the test to tell whether the 2nd 64K is bad, or not present. For this reason, it is possible to view the detailed test results after the test passes, as well as after a failure.

There are up to eight screens of data presented as detailed test results for the Wave Memory test. The first two screens present interrupt counts and ROM checksums for DSP 1. The third screen presents the first page of RAM checksums. If there are more RAM checksums applicable for the type of memory chips being tested, then the next three pages will show the remaining RAM checksums. The last two screens present the results of the test performed by DSP 2. This will help to narrow down any problem with one of the DSP chips. The tests run by each DSP are identical, except that DSP 2 does not compute checksums for Sample RAM.

NOTE: that the 'RAM addressing jumper' is part of the addressing hardware, and must be reconfigured for different RAM sizes. For 28-pin RAM chips, the jumper should be positioned closest to the main processor board connectors; for 32-pin RAM chips, the jumper is placed farthest from the main processor board. For the 1990 Memory board, there are two jumpers. They must always be moved together. If one jumper is in the 32-pin chip position, then the other jumper must be also. There is no provision for mixing 28-pin with 32-pin RAM chips.In each set of results screens, the results can be interpreted as follows:

1) For the first screen of the set,

int:xxxxxx	Lo cksum: xxxx	DSPx
SSI:xxxxxx	SSI data: xxxxxx	-more-

a) On the far left of the first screen is an interrupt status for the applicable DSP chip. If either 'ints' or 'SSI' contains a value other than 'O.K.', there may be a problem with the DSP chip. A signed numerical value in this field denotes a deviation in the number of interrupts received during the test compared to the expected number of interrupts. Any deviation is an indication of a problem with the DSP or with the clock crystal.

b) In the center of the screen, on the top line is the checksum for the Low Byte of Sample RAM. This byte is unused, and the checksum should always be zero.

c) In the center of the screen, on the bottom line is a data word used in checking the SSI interrupts. If it matches the expected data word, 'O.K.' is displayed. Any other value means that there may be a problem with the relevant DSP chip, or a clock crystal may be out of tolerance.

d) The DSP chip (1 or 2) to which this set of results applies is displayed in the top right hand corner of this screen.

2) For the remaining screens,

ROM	HI: xxxx xxxx xxxx xxxx	
sums	LO: xxxx xxxx xxxx xxxx	-more-

(RAM screens are for DSP 1 only)

RAM1	HI: xxxx xxxx xxxx xxxx	
sums	LO: xxxx xxxx xxxx xxxx	-more-

(RAM checksum pages 2-4 are presented only when 32-pin [128K X 8] memory chips are in use.)

RAM2	HI: xxxx xxxx xxxx xxxx	
sums	LO: xxxx xxxx xxxx xxxx	-more-

(Pages 3-4 are presented only for the 1990 memory board.)

RAM3	HI: xxxx xxxx xxxx xxxx	
sums	LO: xxxx xxxx xxxx xxxx	-more-

RAM4	HI: xxxx xxxx xxxx xxxx	
sums	LO: xxxx xxxx xxxx xxxx	-more-

a) The checksums for each chip are displayed. If a checksum for any portion of memory matches the expected checksum, then 'O.K.' is displayed in the applicable field. Otherwise, the actual (wrong) checksum is displayed in hexadecimal.

b) For the ROM checksum screen, the interpretation depends on which memory board is in use.

For the 1989 board, the first pair (HI,LO) of checksums represent the WaveROM 1 set of chips (WaveROM Hi 1, and WaveRAM Lo 1, respectively). Likewise, the second pair of checksums represent the two WaveROM 2 chips, and so on.

For the 1990 board, the first two pairs of checksums represent the WaveROM 1 set of chips. The third and fourth pairs of checksums represent the two WaveROM 2 chips.

c) The RAM checksums are interpreted slightly differently, depending on which memory board is installed and how much RAM is installed in the board. See figure 1 for the 1989 memory board, and figure 2 for the 1990 memory board.

d) If there are any checksums which are not 'O.K.', they represent problems in some memory area within the relevant chip, unless the values are '0000' or 'FFFF', which likely represents failure of the entire chip.

512K Expandable (1989) Memory Board:

a) If the RAM chips installed are 28-pin, 32k by 8 bit chips (used for 64K and 128K installations), then:

The first set of checksums represent the WaveRAM 1 chips, and the second set of checksums represent the WaveRAM 2 chips.

```
RAM HI:  RAM1  RAM2
sums LO: RAM1  RAM2                -more-
```

b) If the RAM chips are 32-pin, 128K by 8 bit chips (used for 256K and 512K installations), then:

The entire first page of checksums represent the WaveRAM1 chips, and the second page of checksums represent the WaveRAM2 chips.

```
RAM1 HI:  RAM1 RAM1 RAM1 RAM1
sums LO:  RAM1 RAM1 RAM1 RAM1   -more-
```

```
RAM2 HI: RAM2 RAM2 RAM2 RAM2
sums LO: RAM2 RAM2 RAM2 RAM2    -more-
```

Figure 1. 1989 Memory Board Checksums

1 Meg Expandable (1990) Memory Board:

a) If the RAM chips installed are 28-pin, 32K by 8 bit chips (used for 64K, 128K, 192K, and 256K installations), then:

The first set of checksums represent the WaveRAM 1 chips, and the second set of checksums represent the WaveRAM 2 chips. The third set of checksums represent the WaveRAM 3 chips, and the fourth set represent the WaveRAM 4 chips.

```
RAM  HI:  RAM1 RAM2 RAM3 RAM4
sums LO:  RAM1 RAM2 RAM3 RAM4     -more-
```

b) If the RAM chips are 32-pin, 128K by 8 bit chips (used for 256K, 512K, 768K, and 1 Meg installations), then:

The entire first page of checksums represent the WaveRAM1 chips, and the second page of checksums represent the WaveRAM2 chips. The third page represents the WaveRAM3 chip pair, and the fourth page represents the WaveRAM4 pair.

```
RAM1 HI:  RAM1 RAM1 RAM1 RAM1
sums  LO: RAM1 RAM1 RAM1 RAM1     -more-
```

```
RAM2 HI:  RAM2 RAM2 RAM2 RAM2
sums  LO: RAM2 RAM2 RAM2 RAM2     -more-
```

```
RAM3 HI:  RAM3 RAM3 RAM3 RAM3
sums  LO: RAM3 RAM3 RAM3 RAM3     -more-
```

```
RAM4 HI:  RAM4 RAM4 RAM4 RAM4
sums  LO: RAM4 RAM4 RAM4 RAM4     -more-
```

Figure 2. 1990 Memory Board Checksums

EXAMPLES:

1) Upgrading the Wave RAM in the 1989 memory board from 64K to 512K without changing the RAM addressing jumper would result in the following screens:

```
                Wave mem Test: PASSED
-more-          256K RAM approved.          -ret-
```

We're expecting to see '512K RAM approved', so we choose -more- to see what's wrong.

```
int:O.K.        Lo cksum: 0000              DSP1
SSI:O.K.        SSI data: O.K.              -more-
```

```
ROM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.             -more-
```

```
RAM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.             -more-
```

```
int:O.K.        Lo cksum: 0000              DSP2
SSI:O.K.        SSI data: O.K.              -more-
```

```
ROM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.             -more-
```

Notice that only one page of RAM checksums is displayed, indicating that the test thinks it is dealing with 28-pin RAM chips. Remember that part of the addressing hardware, the RAM addressing jumper, must be reconfigured for different RAM sizes.

The solution to this problem is to move the jumper from the 28-pin chip position to the 32-pin chip position (farthest from the main processor board connectors).

2) Contamination of the contacts of the "DSP 1" chip might result in the following screens:

```
int:O.K.        Lo cksum: 0000              DSP1
SSI:O.K.        SSI data: O.K.              -more-
```

```
ROM     HI: 8821 A14C B429 455A
sums    LO: BC39 B31C A69A DF24             -more-
```

```
RAM1    HI: 2E10 2E10 43E0 43E0
sums    LO: E960 E960 5680 5680             -more-
```

```
RAM2    HI: 59F0 59F0 E480 E480
sums    LO: BFC0 BFC0 3BE0 3BE0             -more-
```

```
int:O.K.        Lo cksum: 0000        DSP2
SSI:O.K.        SSI data: O.K.        -more-
```

```
ROM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.       -ret-
```

Noting that all of the checksums for DSP 2 are good, while those for DSP 1 are bad, we know that there is a problem with DSP 1.

The solution to this problem is to remove "DSP 1" (using the correct tool only!), and clean it or replace it.

3) A crushed data pin on a 28-pin Wave RAM chip added to expand memory from 64k to 128k (on the 1989 Memory board) would result in the following screens (or something similar):

```
                Wave mem Test: PASSED
-more-          64K RAM approved.       -ret-
```

Since we should have 128K of RAM after the upgrade, we choose -more- to see what's wrong.

```
int:O.K.        Lo cksum: 0000        DSP1
SSI:O.K.        SSI data: O.K.        -more-
```

```
ROM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.       -more-
```

```
RAM     HI: O.K. O.K.
sums    LO: O.K. 155C                 -more-
```

```
int:O.K.        Lo cksum: 0000        DSP2
SSI:O.K.        SSI data: O.K.        -more-
```

```
ROM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.       -more-
```

```
RAM     HI: O.K. O.K. O.K. O.K.
sums    LO: O.K. O.K. O.K. O.K.       -ret-
```

The checksum corresponding to the "WaveRAM Lo 2" chip is not 'O.K.' Looking at the chip, we see that one lead was crushed during insertion.

The solution to this problem is to remove the "WaveRAM Lo 2" chip, straighten the bent pin, and carefully re-insert the chip.

4) Internal failure of the DSP 2 chip might result in the following screen:

Wave mem Test: DSP2 com ERR
-more- -ret-

The solution to this problem is to replace DSP 2.

E) BATTERY

If the System Battery voltage is low, the battery could need recharging. For a machine which has been in regular use, the battery should stay charged for up to nine months of storage. If the DPM 3 has not been turned on for more than nine months, simply leaving the machine "on" overnight should restore battery voltage to an acceptable level. If recharging does not bring the voltage up to an acceptable level, the battery should be replaced.

If the Cartridge Battery is low, then the battery in that cartridge should be replaced.

F) MIDI

If the MIDI Test fails, two possible remedies are:

1) Replace the Opto-isolator.

2) Replace the MIDI UART.

G) FRONT PANEL

When the Front Panel test is selected, it takes about three seconds to initialize the Front Panel Processor for test mode. At this point, all of the switches and switch lines will be checked for shorts. If a shorted switch is found, a message saying so will be displayed and the test will be terminated. Note that pressing any switches during this test period will interfere with the test, and may be interpreted by the test as shorts in the switch hardware!

Once Front Panel Test initialization is complete, the view angle of the display (LCD) can be adjusted by holding down any two switches (with the exception of the switches that select tests), and rotating the data wheel.

To run one of the front panel tests, simply select the desired test with the button corresponding to that test. Choices available are the SWITCH TEST, ANALOG DEVICE TEST, and DATA WHEEL TEST. The SERIAL I/O TEST is intended for factory service technicians only.

After a test is run, the test mode menu will again be displayed. This allows the user to run tests over again if necessary.

Following is a detailed explanation of each test.

1) SELF DIAGNOSTICS DURING TEST MODE INITIALIZATION

During the three second delay encountered after selecting 'Front Panel' test from the main diagnostics menu, the Front Panel tests itself to see if any of the switches and associated circuit board traces are shorted. If a short is found, a message will be put on the LCD saying so. Even though the message says that a shorted switch was found, it could also be a solder short or a component lead short, etc. Therefore, it is important to check the solder side of each board for shorts before assuming that a switch itself is bad.

2) SWITCH TEST

Select the SWITCH TEST using the leftmost softkey under the display. The switch test is activated immediately. Any time a switch closure is detected, the location is displayed on the LCD and will remain displayed until another switch is detected.

If two switches are detected, then both locations will be displayed. Both detected switch closures remain on the LCD until another switch is detected. Three switch closures are not allowed; therefore, the third switch will not be detected.

If a switch is pressed and the closure is not detected, the location of the last switch detected will remain on the display. This would indicate that either a switch send/return line is open, or the switch is bad.

A single switch press should show a single closure. If a single switch press causes a double switch closure to be displayed, then there is a shorted condition in the front panel circuit or cables.

Before replacing a switch, make sure the ribbon cable connecting the boards is secure and no traces are open. A continuity tester is all that is needed to find an open trace.

The Switch Test allows 64 switch closures before returning to the main menu. All the switches should be checked, as well as a reasonable sampling of several switch pairs.

3) ANALOG DEVICE TEST

Select the ANALOG DEVICE TEST with the center left soft key. To check each analog device, simply move the device. If everything is working properly, the device code and value will be displayed. The value displayed will change by 2 as the device is moved. Device codes are shown in figure 3.

For the Volume Pedal, Volume Slider, Data Entry Slider, and After-Touch Sensor, the ideal values would range between 0 and 255, but, because of real world tolerances, the actual values are typically between 0 and 253.

For the Pitch Wheel, the center value should be approximately 120. The range of values should be a minimum of +/- 39 from center.

For the Modulation Wheel, the minimum value must be less than 80. Again, the 'center' value should approximate 120.

Analog Device Codes

DEVICE NUMBER	DEVICE NAME
130	Volume Pedal
131	Volume Slider
132	Data Entry Slider
133	Modulation Wheel
134	Pitch Wheel
135	After-Touch Sensor

Figure 3. Analog Device Codes

Should the display not reflect the proper device and/or value, some troubleshooting is in order. Check to make sure all the cables that connect the pitch wheel, modulation wheel, and aftertouch strip are secure. If there is no evidence of a problem with the cables, the problem is probably on the front panel processor board.

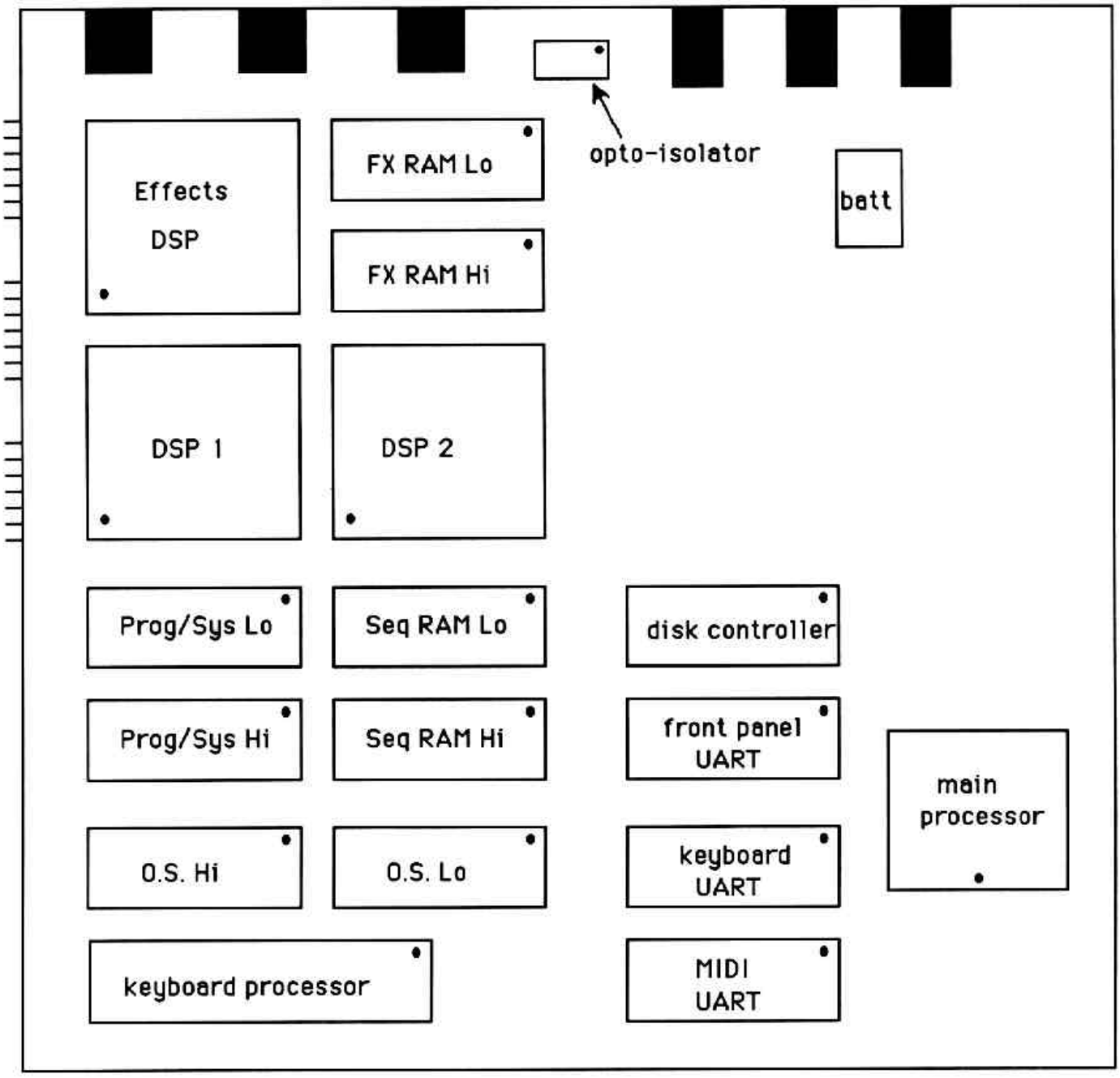
The Analog Device Test will time out after no movement is detected for several seconds, and the main menu will return.

4) DATA WHEEL TEST

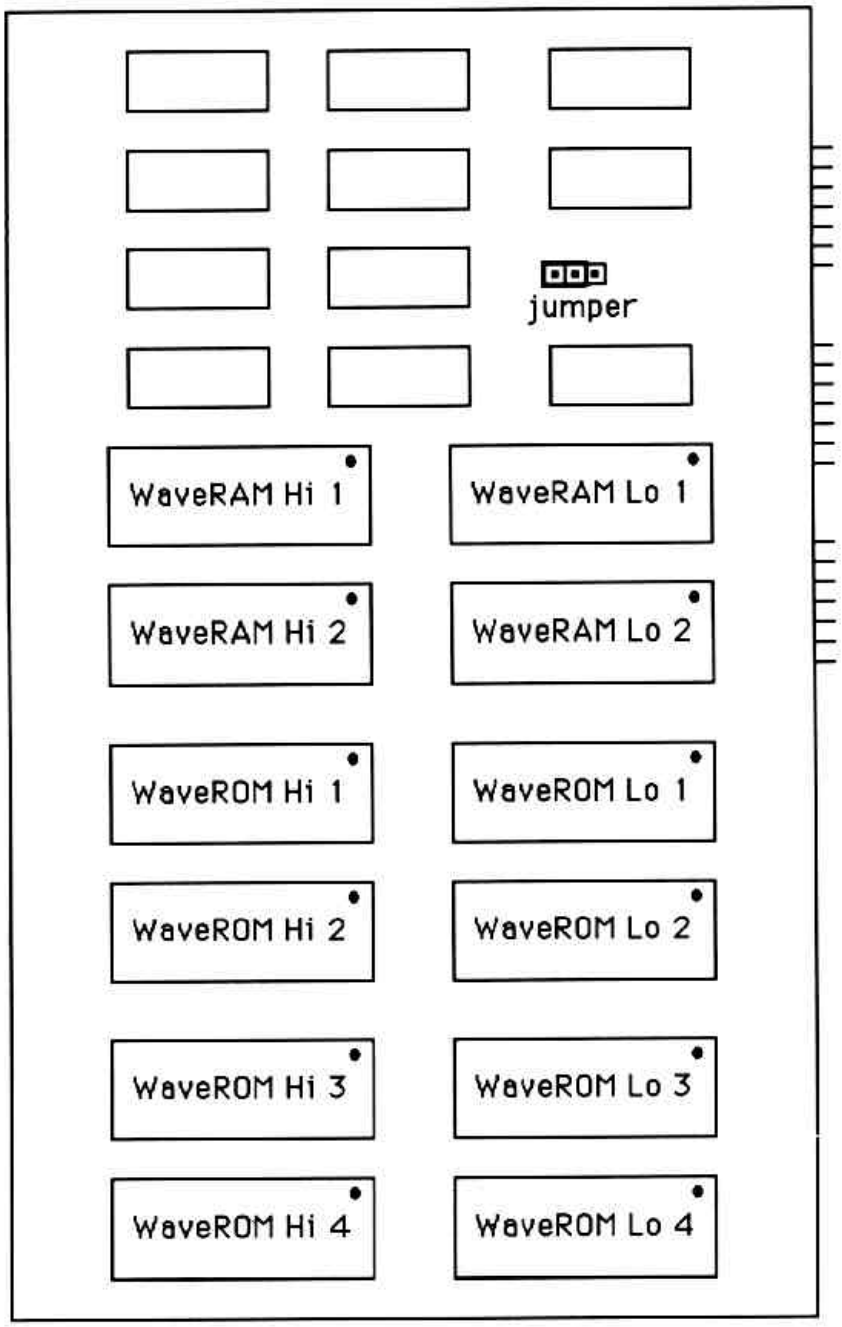
Select this test with the center right softkey. Move the data wheel clockwise (CW) and counterclockwise (CCW). The value displayed (0-255) should be incremented for clockwise movement, and decremented for counterclockwise. If there is no response, check the connections on the cable before doing anything else.

The Data Wheel Test will allow 512 values to be displayed before returning to the main menu.

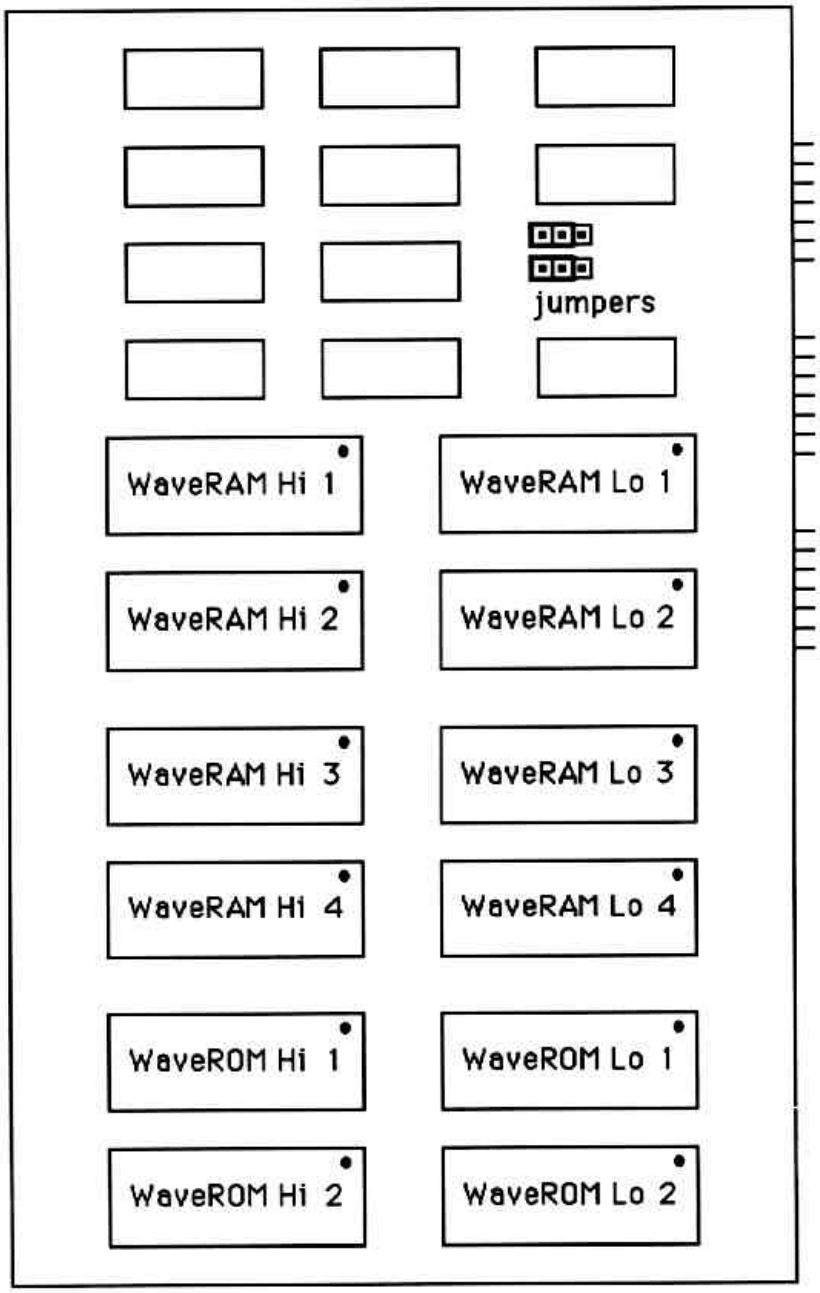
APPENDIX A



DPM-3 Main Processor Board



DPM-3 Memory Board (1989)



DPM-3 Memory Board (1990)

Features and specifications subject to change without notice.

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